CEZAMAT
WARSAW UNIVERSITY OF TECHNOLOGY

SEMINSYS
PACKAGING & ASSEMBLY

PACKAGING & ASSEMBLY SERVICES

FROM FABRICATED WAFER TO PACKAGED DEVICE

Electronic and photonic chip packaging

R&D
PROTOTYPING

TECHNOLOGY
TRANSFER

SMALL-VOLUME
PRODUCTION

ADVANCED SEMICONDUCTOR, MICROELECTRONIC AND PHOTONIC PACKAGING

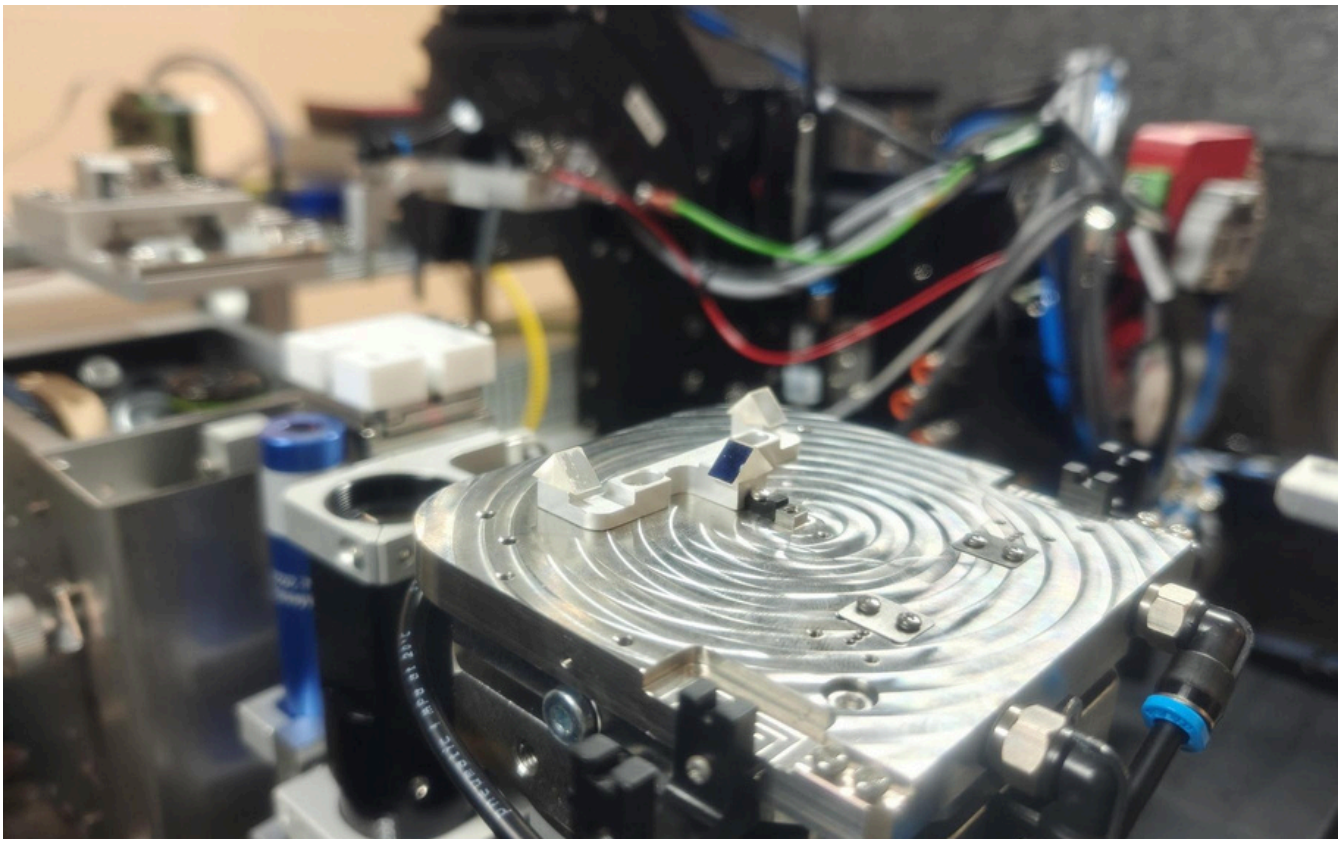
01 · INTEGRATED ENVIRONMENT

Integrated packaging across the full process chain

CEZAMAT provides an integrated environment for advanced semiconductor, microelectronic, and photonic packaging, covering the full chain from wafer preparation through assembly to characterization.
A key strength is the development and optimization of customized processes for non-standard materials, device architectures, and research applications, with optical, electrical, and mechanical characterization integrated directly into process development and validation.

The infrastructure is well-suited to R&D, prototyping, technology transfer, and small-volume production.

WAFER PREPARATION — ASSEMBLY & INTERCONNECT — CHARACTERIZATION & VALIDATION



02 · CORE CAPABILITIES

Wafer preparation and high-precision assembly

01

Wafer dicing

Wafer dicing — Full-cut, partial-cut, step-cut, and ultrasonic dicing of silicon, glass, sapphire, GaN, SiC, and other substrates, with parameters adapted to material, wafer thickness, and device geometry.

02

Thinning and integrated wafer processing

Backgrinding and fine grinding of wafers up to 200 mm diameter to a specified final thickness; dicing before grinding (DBG); post-process cleaning and handling on dicing frames.

03

Die attach and flip-chip assembly

Sub-micron placement of dies, PICs, and microcomponents in face-up, face-down, chip-to-chip, and chip-to-substrate configurations, using adhesive/UV, solder, and eutectic, thermocompression, and thermosonic bonding; pressure-assisted Ag sintering for SiC and GaN power devices.

04

Solder bumping and laser joining

Fluxless laser solder ball jetting and reflow for localized soldering, bump formation, and flip-chip interconnection; localized laser soldering with visual and infrared alignment for low thermal load.

03 · CORE CAPABILITIES - CONTINUED

Interconnection, photonic integration and validation

05

Wire and ribbon bonding

Ball-wedge and wedge-wedge bonding with Au, Al, and Cu fine wire and Au ribbon; heavy aluminum and Cu-core wire for high-current power modules; manual bonding, rework, and deep-access or non-standard geometries.

06

Photonic integration and active alignment

Hybrid assembly of PICs, lasers, photodiodes, and electronic ICs; automated multi-axis alignment with real-time optical and electrical feedback; fiber and fiber-array attach with precision adhesive dispensing and UV curing; micro-optics handling and alignment.

07

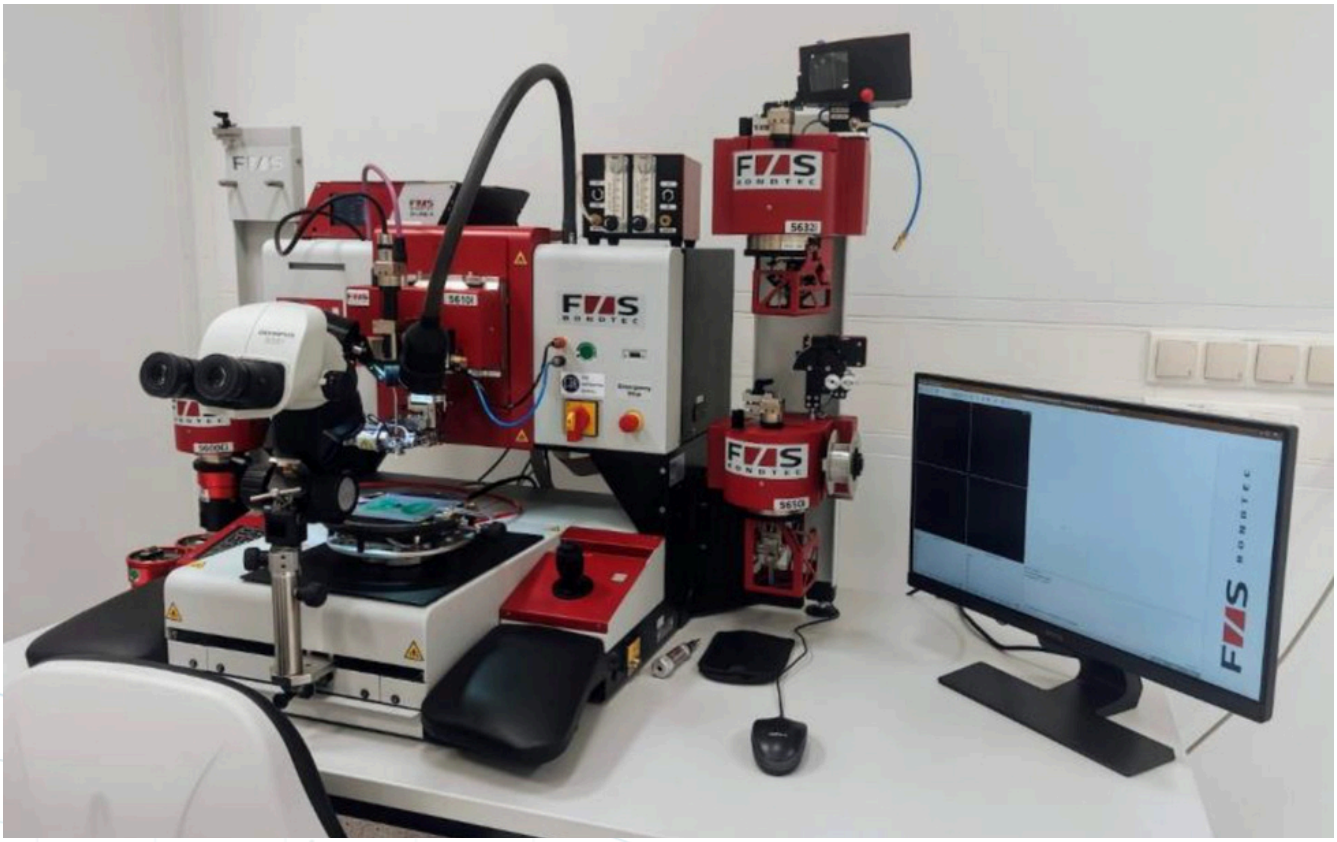
Hermetic sealing

Precision laser welding of metal packages in a controlled nitrogen or argon atmosphere, with helium leak-tightness capability, for sensitive electronic, photonic, and MEMS devices.

08

Characterization and process development

Pull and shear testing of die attach, wire, and ribbon bonds; development and optimization of complete assembly and interconnection sequences, feasibility studies, rework, and small-batch microassembly.



04 · ENGAGEMENT

From inquiry to packaging and reporting

TYPICAL USE

Development and validation of packaging processes for semiconductor, power electronic, photonic, optoelectronic, sensor, and MEMS devices, including feasibility studies, prototype fabrication, process optimization, rework, and small production series.

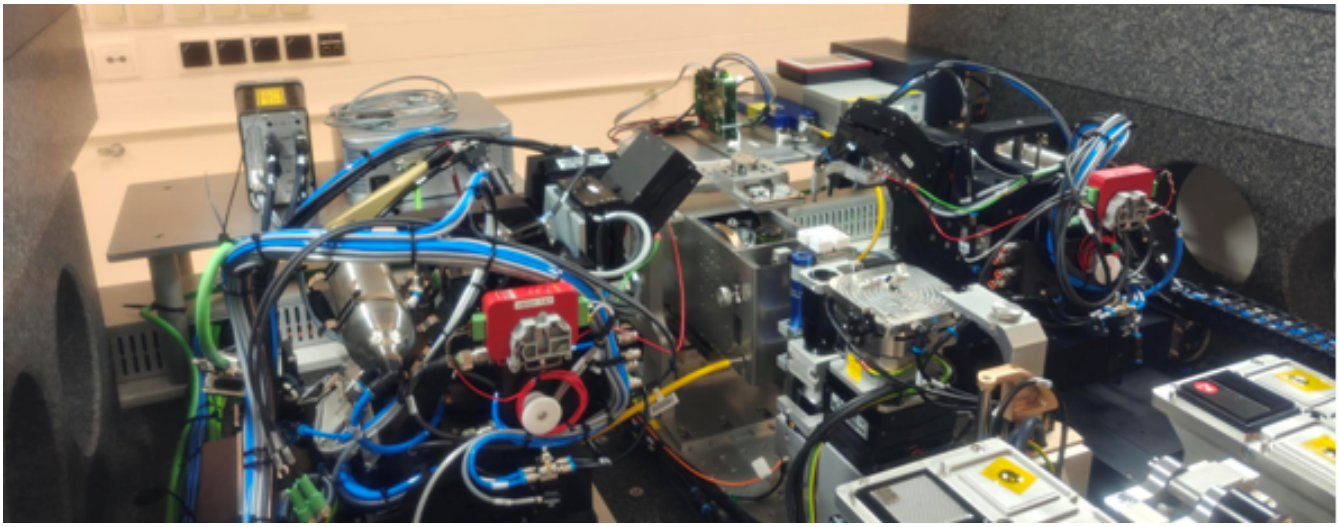
YOU PROVIDE

Devices, wafers, substrates, materials, and any available technical documentation required to define the target assembly or processing sequence.

HOW TO ENGAGE

7 - STEP PROCESS

1. Inquiry
2. NDA
3. Feasibility assessment
4. Quotation
5. Order & sample delivery
6. Packaging
7. Report



Scope note

The exact process flow, achievable parameters, and required materials are defined individually for each project and depend on device design, material compatibility, and application requirements. Non-standard processes and materials may require preliminary feasibility tests and dedicated process development.

05 · CONTACT

Let’s define the right packaging process

Discuss your device, material system, target architecture, and validation requirements with the CEZAMAT SEMINSYS team.

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