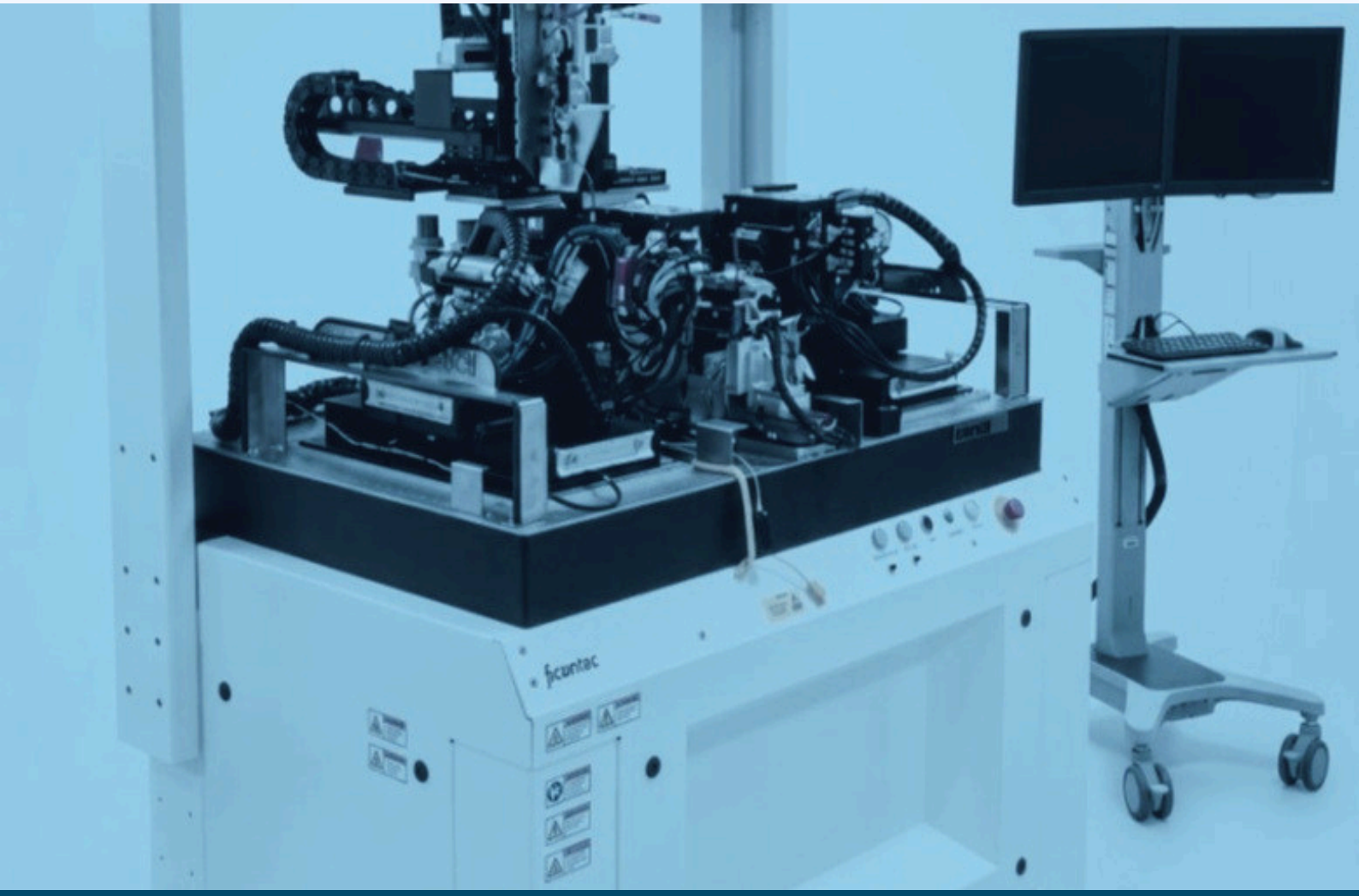


PHOTONIC & ELECTRONIC CHARACTERIZATION

FROM FABRICATED CHIP TO MEASURED PERFORMANCE

Photonic characterization with complementary electrical measurements

ACTIVE & PASSIVE PICS

VISIBLE & C-BAND

OPTICAL & ELECTRICAL MEASUREMENTS

RAW DATA & PROCESSED RESULTS

MEASURED EVIDENCE FOR DESIGN VALIDATION, PROCESS FEEDBACK AND PACKAGING DECISIONS

01 · INTEGRATED ENVIRONMENT

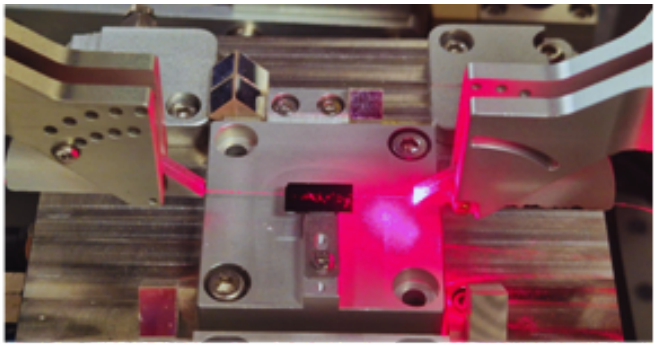
Measured evidence at chip level

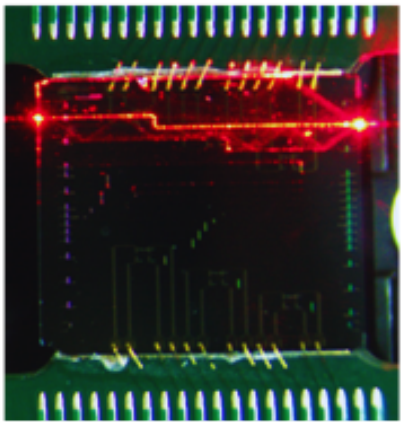
You have photonic chips and need measured evidence of their behavior.
We measure active and passive PICs at chip level across the visible spectrum and C-band, using edge and vertical coupling, and deliver raw data together with processed results.

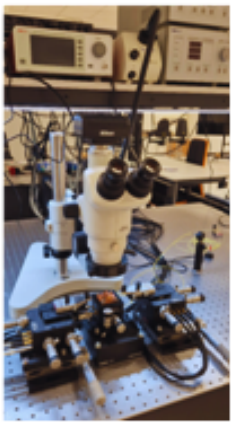
Measurement is co-located with PIC design and fabrication, enabling discrepancies to be traced back to layout or process without moving the chip to another organization. Chips fabricated elsewhere are accepted, subject to feasibility assessment.

CHIP-LEVEL MEASUREMENT	DESIGN & PROCESS FEEDBACK	EXTERNAL CHIPS ACCEPTED*

* Subject to feasibility assessment.







02 · PHOTONIC CHARACTERIZATION CAPABILITIES

What we measure and how we deliver results

1 **Passive spectra**
Insertion and coupling loss; Q, FSR, finesse, and extinction ratio.

2 **Polarization-resolved characterization**
PDL, PMD/DGD, TE/TM loss and Jones and Mueller matrices.

3 **Active devices**
L-I-V, efficiency and threshold; optical coupling and electrical probing on one station.

4 **Series measurement**
Programmable routines on the ficonTEC T300; high port counts, arbitrary orientation.

5 **Bespoke measurement**
Reconfigurable piezo-stabilized setups for non-standard geometries and single structures.

6 **Campaign design and reporting**
Agreed measurement plan; PDF and CSV.

TYPICAL USE

01. Lot acceptance - for our line or a third-party foundry.	**04.** Coupling-loss budgeting ahead of packaging.
02. Design validation against models, feeding back into PDK development.	**05.** Visible-band circuits.
03. Resonant structures for filters, delay lines and sensing.	**06.** Prototype and short-series support.

03 · ELECTRICAL CHARACTERIZATION

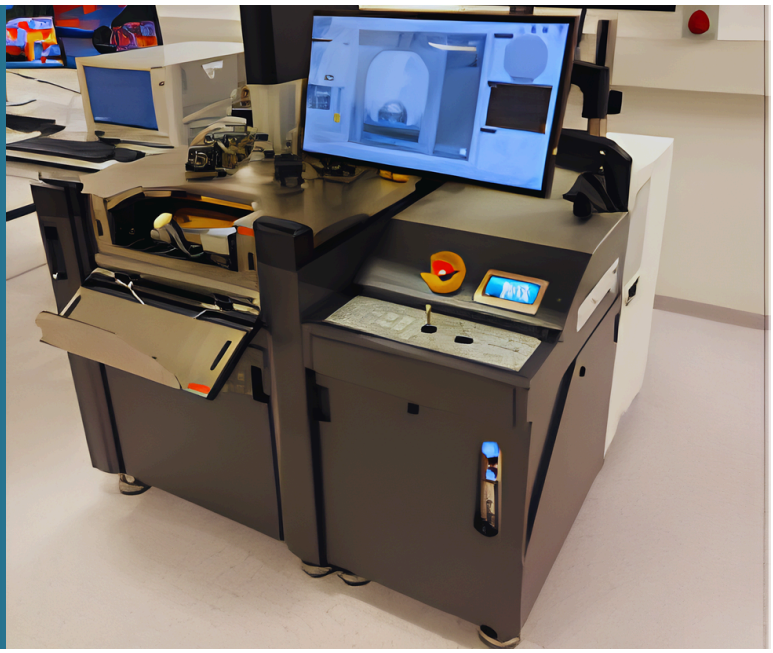
Electrical evidence alongside photonic results

For devices that require both optical and electrical evidence, CEZAMAT can complement chip-level photonic measurements with on-wafer and discrete-device electrical characterization.

200 mm
on-wafer probing

−60 to 300 °C
chuck temperature range

10 fA
current resolution



INTEGRATED ENVIRONMENT
Electrical measurement is available on the same site as design, processing and packaging, supporting faster interpretation of device behaviour.

On-wafer probing is available up to 200 mm. Discrete devices can be measured with up to four terminals, while circuits can be measured with up to six. The infrastructure includes semi-automatic and manual probe stations, a semiconductor parameter analyzer, source-measure units and an impedance analyzer.

ON-WAFER	DISCRETE DEVICES	CIRCUITS
up to 200 mm	up to 4 terminals	up to 6 terminals

04 · ELECTRICAL MEASUREMENT CAPABILITIES

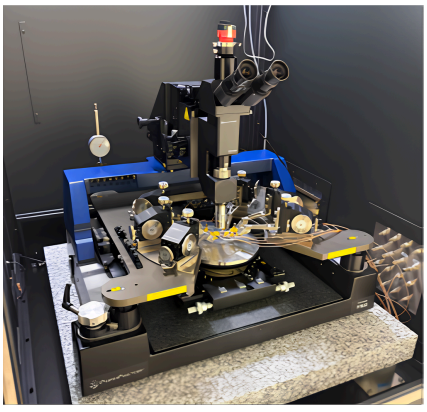
What we measure

1 **I–V characterization**
100 V / 1 A on wafer; 200 V / 3.3 A for discrete devices. Lowest ranges: 25 µV and 50 fA.

2 **Pulsed measurement**
Programmable pulses from 100 ns with 10 ns current resolution; 0–10 V in 10 mV steps, ranges 1 µA to 10 mA.

3 **Small-signal and impedance**
20 Hz to 20 MHz, including impedance spectroscopy and equivalent-circuit fitting.

4 **Automation**
Programmable automated measurement of every circuit on a wafer; deviation mapping across wafer.



Electrical characterization is available on the same site as design, processing and packaging.

03 · ENGAGEMENT

From inquiry to measurement and reporting

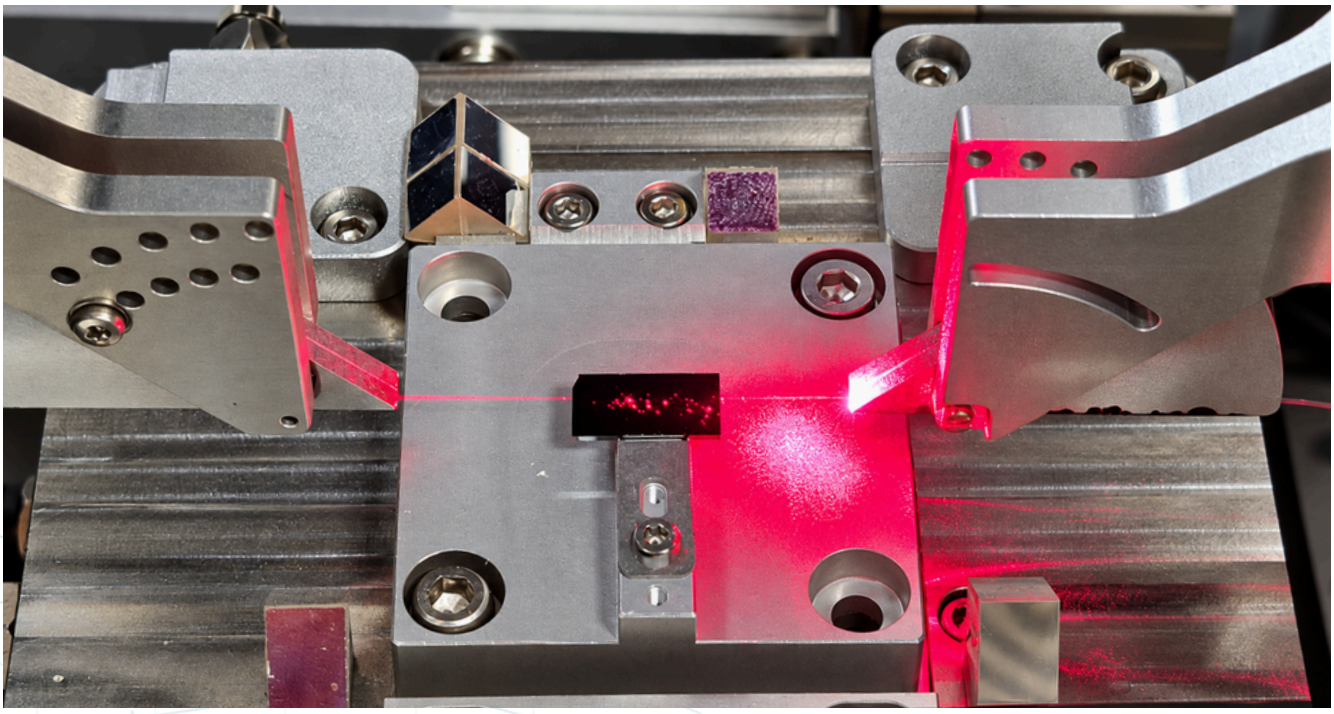
YOU PROVIDE

1	Device description and chip count
2	Port layout and orientation
3	GDS with port labeling
4	Target spectral range and parameter list
5	For active devices: pinout, bias and drive limits, and damage thresholds

HOW TO ENGAGE

7 - STEP PROCESS

1 Inquiry → 2 NDA → 3 Feasibility assessment → 4 Quotation → 5 Order & sample delivery → 6 Measurement → 7 Report



04 · SCOPE AND CONTACT

Clear service boundaries - Actionable results

Scope note

The service is focused on chip-level photonic characterization.
The following activities are outside the offered scope:

1	Wafer-level optical probing
2	High-speed opto-electronic characterization: S21, eye and BER
3	Reliability, environmental or radiation testing
4	Qualification to ECSS, ESCC, MIL-STD-883 or Telcordia standards

DELIVERABLES ARE TECHNICAL MEASUREMENT REPORTS

NEXT STEP

Discuss your photonic measurement requirements with us.
Share your device description, chip count, port layout and target spectral range.
We will assess feasibility and define the appropriate measurement plan.

CONTACT	SERVICE
CEZAMAT Warsaw University of Technology **seminsys@pw.edu.pl** **marcin.lelit@pw.edu.pl**	Chip-level photonic characterization **Active and passive PICs · Visible spectrum and C-band · Raw and processed results** Electrical characterization **Device level electrical characterization · DC measurements · Pulse measurements · Small-signal characterization · Statistical measurements and analysis**