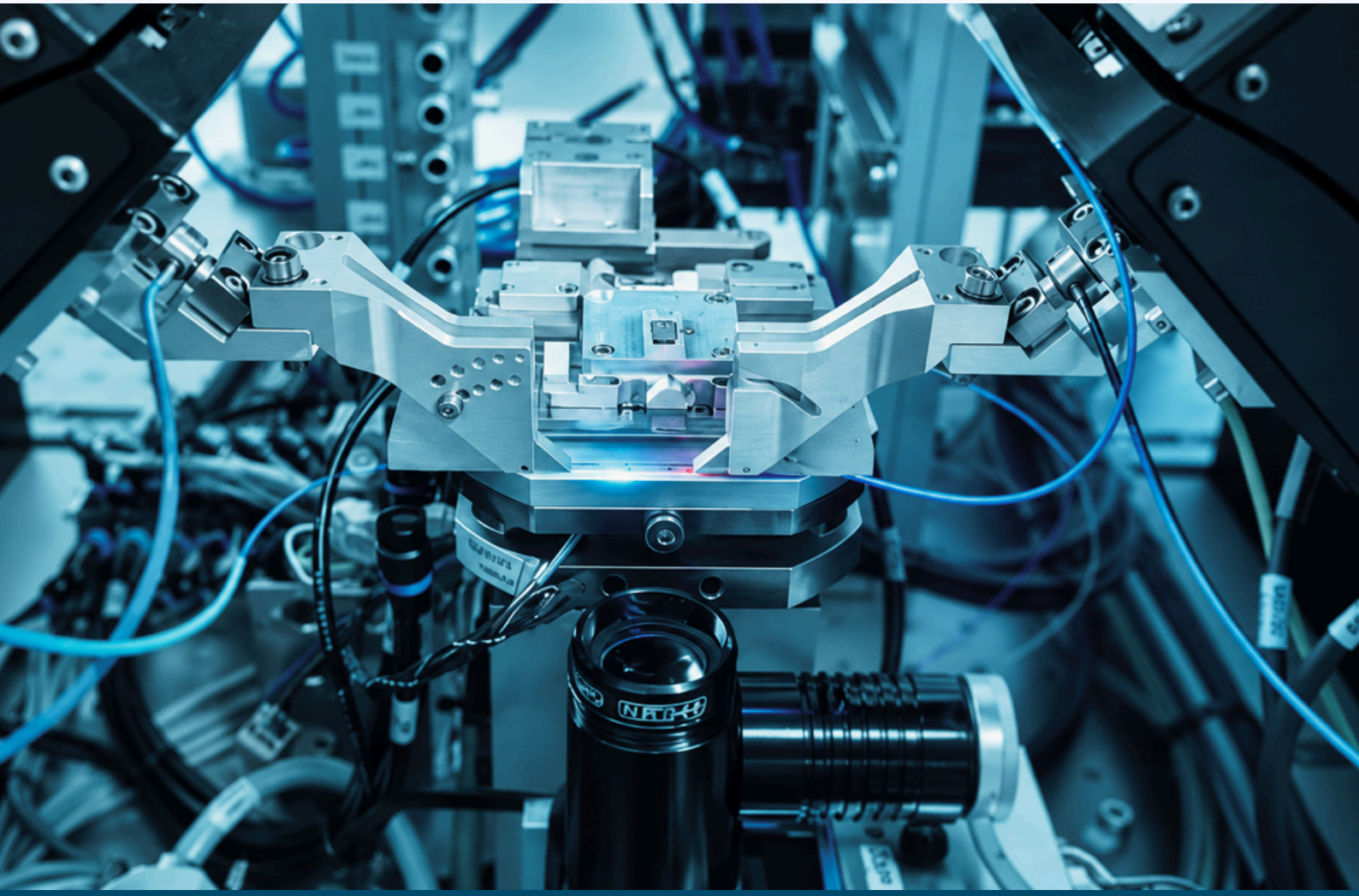
CEZAMAT
WARSAW UNIVERSITY OF TECHNOLOGY



PHOTONIC DESIGN AND MODELING

FABRICATION-READY PIC DESIGN

Photonic device modeling, circuit simulation and PIC design

DEVICE MODELING

CIRCUIT SIMULATION

PIC LAYOUT

DESIGN VERIFICATION

A FOCUSED SERVICE. AN INTEGRATED ENVIRONMENT

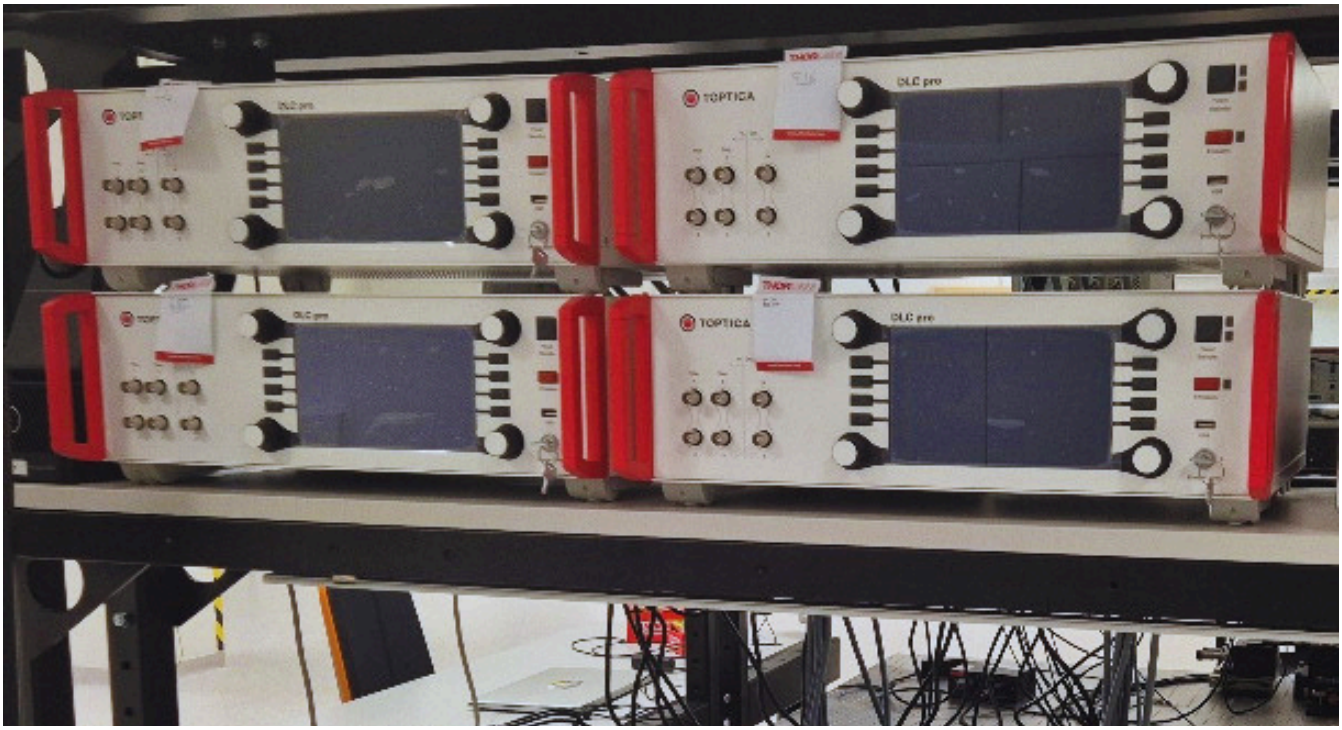
01 · INTEGRATED ENVIRONMENT

Design intent connected to fabrication reality

From a device concept to a layout ready for fabrication.
We model photonic devices and design the circuits built from them - as a standalone service, or as the entry point of a chain that continues at the same site into fabrication, photonic assembly and characterization.

Designs are produced on our own SiN PDK or on external partner PDKs. The design team and process team sit in one department, so design intent is checked against the process window of the line that will build the circuit.

STANDALONE SERVICE — CEZAMAT SiN OR EXTERNAL PDK — DESIGN & PROCESS IN ONE DEPARTMENT



DEVICE CONCEPT — MODELING — CIRCUIT SIMULATION — PIC LAYOUT — FABRICATION READY DELIVERY

02 · CORE CAPABILITIES

Device modeling and circuit-level simulation

WHAT WE DELIVER

01 **Device modeling**
FDTD, eigenmode, BPM, multilayer, heat and charge.

02 **Circuit simulation with compact models**
Circuit-level simulation using compact models and S-parameters.

03 **PIC layout on the CEZAMAT SiN platform**
Standard cells and design rules; GDS delivery.

04 **PIC design on external-partner PDKs**
Passive, active, hybrid.

05 **Verification of a client-supplied design**
Against target-platform design rules and pilot-line process constraints.

06 **Micro-optical and diffractive elements**
Separate offer.

TYPICAL USE

01. Visible-band SiN circuits around 637 nm	**02.** Sensing PICs
03. Pre-tape-out design review, including an independent manufacturability opinion on an existing layout	**04.** Micro-optics and DOEs

03 · ENGAGEMENT

From inquiry to a fabrication-ready delivery

YOU PROVIDE

1	Intended circuit functionality
2	Target platform and band
3	Parametric requirements (loss, bandwidth, extinction, footprint, thermal and electrical interfaces)
4	Expected deliverables
5	For verification: GDS, design intent, and the design-rule deck the layout was drawn against

HOW TO ENGAGE

6 - STEP PROCESS

1 Inquiry → 2 NDA → 3 Feasibility assessment → 4 Quotation → 5 Order → 6 Delivery*

*Delivery of GDS, compact models, simulation report, design documentation

Scope note

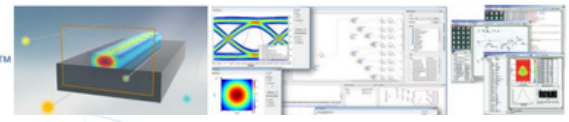
No MPW service; commission only. No CMOS design — the line has no projection lithography, no multi-level BEOL. C-band SiN library in preparation, not committable to a schedule.

DESIGN AND MODELING ENVIRONMENT

Ansys part of SYNOPSYS

Optiwave DESIGN SOFTWARE

Nazca design™ photonic IC design framework



04 · CONTACT

Let's develop the right photonic design path

Discuss your circuit functionality, target platform, operating band and required deliverables with the CEZAMAT SEMINSYS team.

CONTACT	SERVICE
CEZAMAT Warsaw University of Technology **seminsys@pw.edu.pl**	Photonic modeling and design **Device modeling · Circuit simulation** **PIC layout · Design verification**

MODEL **SIMULATE** **LAYOUT** **VERIFY** **DELIVER**